REMARKS

Claims 1-4, 6-11, 13-14, 21-24, and 26 are all the claims presently pending in the application. Claims 5, 12, 15-20, and 25 have been cancelled without prejudice or disclaimer. Claims 1, 8, and 21 have been amended herein. Claims 1-14 and 21-26 as well as the drawings have been rejected. Applicants respectfully traverse these rejections based on the following discussion.

I. The Objections to the Drawings

The drawings are objected to under 37 C.F.R. §1.83(a). According to the Office Action, the features of a thermal material between a top of the memory chip package and a bottom of an adjacent substrate, as recited in claims 6, 13, and 26; and the features of the space between a top of the memory chip package and a bottom of the adjacent substrate being greater than a height of the memory chip package, as recited in claim 21 must be shown or the feature(s) canceled from the claim(s).

Applicants note that such features are clearly shown in Figure 1. Specifically, a thermal material 160 are clearly shown between a top of the memory chip package 140 and a bottom of an adjacent substrate 120. Furthermore, the gap 122 between a top of the memory chip package 140 and a bottom of the adjacent substrate 120 being greater than a height of the memory chip package 140 is shown in Figure 1. The claims have been amended to refer to the previously recited "space" as the "first gap." In view of the foregoing, the Examiner is respectfully requested to remove the objections to the drawings.

II. The 35 USC §112 Rejections

Claims 21-26 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. According to the Office Action, the specification, as originally filed, does not disclose that a space, which is formed between a top of the memory chip package and a bottom of the adjacent substrate by substrate spacers, is greater than a height of the memory chip package, as recited in claim 21. Applicants respectfully traverse these rejections based on the following discussion. On page 4 of the specification, as filed, it clearly states that "[t]he gap is larger than a height of the memory chip packages." In view of the foregoing, the Examiner is respectfully requested to remove this rejection.

Claims 21-26 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Office Action indicates that there is some confusion as to whether the "gap" and "space" recited in the claims refer to the same or a different element of the invention. As such, Applicants have amended claim 21 to make the distinction clearer, whereby element 122 is the "first gap" and element 121 is the "second gap." That is, the first gap 122 is the gap between a top of the memory chip package 140 and a bottom of an adjacent substrate 120, while the second gap 121 is defined by the connectors 130 having a size sufficient to form a second gap 121 between said substrates 120, wherein the second gap 121 is larger than a height of the memory chip package 140. Moreover, Figure 1 clearly shows each element as well. In view of the foregoing, the Examiner is respectfully requested to remove this rejection.

III. The 35 U.S.C. §102 Rejections

Claims 1, 3 and 7 are rejected under 35 U.S.C. §102(e) as being anticipated by Nakajima (U.S. Patent Application Publication US 2002/0086459), hereinafter referred to as "Nakajima." Nakajima teaches a circuit mounting method and a circuit mounted board which can mount semiconductor elements at a high density. A recessed portion is formed in a board, a memory IC packaged in a chip size package method (CSP) is mounted in the recessed portion, and a memory IC packaged in a thin small outline package method (TSOP) is mounted on the board to cover the recessed portion.

However, amended independent claim 1 is patentably distinguishable from Nakajima. Specifically, the claimed invention recites, "wherein said connectors comprises solder balls arranged in a fine ball grid array." The Office Action indicates that Nakajima teaches connectors 25 of the claimed invention. However, on page 2, paragraph [0030] of Nakajima, it is indicated that the connectors include a male connector 23 and a female connector 25 for engaging one another, thereby connecting one interposer 21 to another. Clearly, these male and female connectors 23, 25 are structurally and patentably distinguishable from connectors 130 of the claimed invention, which are solder balls. In fact, the solder ball connectors 130 form a fine ball grid array (FBGA) as shown in Figure 2. Additionally, Nakajima does not teach a FBGA in this manner.

Furthermore, it would be unobvious to use solder balls arranged in a FBGA with the device shown in Nakajima because Nakajima teaches away from using such an arrangement through their very specific and intentional use of male and female connectors 23/25 to provide readily stackable devices. Furthermore, while Figure 3 of Nakajima shows using solder balls 33b as connectors between substrates, clearly these connectors 33b are not the same as the

claimed invention's substrate spacers 130, which form a second gap between a top of the memory chip package 140 and a bottom of an adjacent substrate 120, wherein the second gap is greater than a height of the memory chip package 140. Clearly in Nakajima the connectors 33b do not provide a gap between the memory chip package and the adjacent substrate, such that the gap is greater than a height of the memory chip package, and any reading into Nakajima teaching this would be purely conjecture and inapposite the drawings and specification of Nakajima. In view of the foregoing, the Examiner is respectfully requested to remove this rejection.

IV. The 35 U.S.C. §103 Rejections

Claims 4-6, 8, 10-14, 21, and 23-26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakajima in view of Miremadi et al. (U.S. Patent No. 5,854,507), hereinafter referred to as "Miremadi." Miremadi teaches a multiple chip assembly where multiple chips are stacked on top of one another using relatively low melting temperature solder balls. Preferably, the chips (either packages or flip chip attachment) are each mounted to a substrate which is larger in lateral surface area than the associated chip. Each substrate thus has a free area, not masked by the chip, which is utilized to mount a vertically-adjacent substrate. Within this free area, solder balls connect the substrates to provide for vertical logic bus propagation through the assembly and vertical heat dissipation. The solder balls are made to have a relatively low melting temperature, permitting interconnection between chip/substrate layers without affecting connection between chip and substrate or with an intervening carrier. At the same time, the layers are compressed together during such interconnection to bring a thermal transport layer in contact between the bottom of each substrate and the chip of an underlying layer, to facilitate lateral heat dissipation.

However, amended independent claims 1, 8, and 21 are patentably distinguishable from Nakajima. Specifically, the claimed invention recites, "wherein said connectors comprises solder balls arranged in a fine ball grid array." The Office Action indicates that Nakajima teaches connectors 25 of the claimed invention. However, on page 2, paragraph [0030] of Nakajima, it is indicated that the connectors include a male connector 23 and a female connector 25 for engaging one another, thereby connecting one interposer 21 to another. Clearly, these male and female connectors 23, 25 are structurally and patentably distinguishable from connectors 130 of the claimed invention, which are solder balls. In fact, the solder ball connectors 130 form a fine ball grid array (FBGA) as shown in Figure 2. Additionally, Nakajima does not teach a FBGA in this manner. Moreover, even if Miremadi were legally combinable with Nakajima, it would still fail to teach all of the elements of the claimed invention.

In fact, Miremadi deals with the use of multiple chips on stacked substrates without providing a gap between the memory chip package and the adjacent substrate. In particular, Figures 8 and 9 of Miremadi clearly show that no such gap exists. In fact, in col. 7, lines 36-39 of Miremadi it states, "[t]his relationship is illustrated by FIG.8, which shows that the bottom side 61 of the first substrate has been brought into direct contact with a top side 62 of the IC 63 of the underlying layer." Thus, the claimed invention is patentably distinct from Nakajima and Miremadi, either alone or in combination with one another.

Claims 2, 9, and 22 are rejected under 35 USC §103(a) as being unpatentable over Nakajima and Miremadi in further in view of Moresco et al. (U.S. Patent No. 5,655,290), hereinafter referred to as "Moresco." Moresco teaches a three dimensional module for housing a plurality of integrated circuit chips. The IC chips are mounted in rows on a plurality of

substrates. Parallel to each row are communications bars, which provide signal paths allowing chips on one substrate to communicate with those on another substrate. The communications bars also serve as spacers between substrates, thereby forming cooling channels. The IC chips are disposed in the cooling channels so that they come into direct contact with the cooling fluid. Signal lines to and from the IC chips are kept as separated as possible from the power lines so as to minimize noise. To this end, relatively thick power supply straps are mounted to each substrate below each row of IC chips. The power supply straps are, in turn, connected to power feed straps such that a very low impedance power supply path to the IC chips is maintained. The overall design of the three dimensional structure is highly modular to facilitate high yield fabrication and repair.

However, amended independent claims 1, 8, and 21 are patentably distinguishable from Nakajima. Specifically, the claimed invention recites, "wherein said connectors comprises solder balls arranged in a fine ball grid array." The Office Action indicates that Nakajima teaches connectors 25 of the claimed invention. However, on page 2, paragraph [0030] of Nakajima, it is indicated that the connectors include a male connector 23 and a female connector 25 for engaging one another, thereby connecting one interposer 21 to another. Clearly, these male and female connectors 23, 25 are structurally and patentably distinguishable from connectors 130 of the claimed invention, which are solder balls. In fact, the solder ball connectors 130 form a fine ball grid array (FBGA) as shown in Figure 2. Additionally, Nakajima does not teach a FBGA in this manner. Moreover, even if Miremadi and Morosco were legally combinable with Nakajima, they would still fail to teach all of the elements of the claimed invention.

Moresco discloses a wholly unique concept from the claimed invention. In Moresco, multiple chips 110 (not chip packages) are stacked on one another, while the claimed invention provides for "a single memory chip package mounted on each of said substrates." An important distinction of the claimed invention is the use of chip scale packages 140. A silicon chip is a rectangular segment of a silicon wafer, consisting of a highly complex active surface, with the bulk of the material being single crystal silicon. Elements of the active surface, important to chip packaging, are primarily the bond pads for electrical connection of the active surface of the chip to the chip package and through the package to the balance of an electronic system. Thus, the claimed invention is patentably distinct from Nakajima, Miremadi, and Moresco, either alone or in combination with one another.

A chip package, shown in Figure 3 of the claimed invention, serves several purposes. The chip package includes a substrate and bond wires that electrically connect pads on the chip to the solder balls. The chip package provides more robust electrical connection features than chip bond pads for the purpose of testing chips. The chip package transforms the chip into a configuration that can be readily and reliably bonded to the next level of assembly, typically a printed circuit board. The chip package offers physical protection to the chip, both against mechanical damage and chemical attack. A chip package may include one or many chips, but is distinguished from higher-level assemblies, such as the one taught in Moresco, in that it directly contacts the chip silicon.

Burn in of multiple chip packages (e.g., packages having more than one chip such as Moresco) also presents difficulties. Wire bondable and over-molded type packages are not reworkable to remove and replace single defective chips. Thus, any failure of a single chip on a multichip package will result either in rework expense or the discard of the balance of still

functional chips on the module. In addition, the functional wiring of a multichip module may make direct testing of a specific function of an individual chip difficult or impossible. Thus, burn in of a multichip module, such as the module taught in Moresco, may be ineffective, and is contrary to the teaching of the claimed invention.

The claimed invention also discloses the use of chip scale package substrates of a size optimized for small size and socket compatibility to permit burn-in for removal of infant mortality defect prior to stack assembly, which simply is not taught, suggested, demonstrated, or achieved in the device described in either Miremadi or Moresco. In fact, the devices of Miremadi and Moresco suggest an over-molded type package, which may not be reworkable to remove and replace single defective chips. Thus, any failure of a single chip on the multichip package of Miremadi or Moresco may result either in rework expense or the discard of the balance of still functional chips on the module in contrast to the claimed invention.

Moreover, because the claimed invention provides chip scale packages 140 that have been "burned-in" and tested, the invention makes the stack out of structures that are known to be "good" (non-defective). This substantially reduces the defect rate for multichip stack decks. Furthermore, because the claimed invention utilizes chips that are known to be free of defects, many more chips can be utilized per deck (e.g., per substrate level) and the number of decks within the stack can be dramatically increased. This is a feature, which the Miremadi and Moresco devices simply do not possess.

Another novel distinction of the claimed invention over Nakajima, Miremadi, and Moresco is that the claimed invention utilizes an optimum number of devices in each stack layer such that the number of independent interconnects required to that layer is minimized. This allows integrated circuit devices to be stacked one upon the other while maintaining a unique pin

out for each pin required in the stack. The number of chips commonly addressed in the stack is expanded to an optimum extent such that the number of memory address interconnects in the stacked module assembly is minimized. In this optimum structure of the claimed invention, the number of data bits addressed in parallel is equal to the system word width. With such a structure as provided by the claimed invention, for each chip added to a deck in the stack structure, an address complement of interconnects needed to expand in the height direction is eliminated. This is a benefit, which the devices in Nakajima, Miremadi, and Moresco do not possess. In fact, the inventive stacked memory module of the claimed invention uses chip scale packaging technology which minimizes the number of solder interconnects between each single chip device and the module circuit board by allowing common addresses in each stack deck. Therefore, the claimed invention achieves efficiency of manufacture by using chip scale packages rather than chips as building blocks at each deck, amenable to standard burn in practices.

Applicants respectfully submit that Nakajima, Miremadi, and Moresco do not teach or suggest the features defined by amended independent claims 1, 8, and 21, and as such, claims 1, 8, and 21 are patentable over Nakajima, Miremadi, and Moresco. Furthermore, dependent claims 2-4, 6-7, 9-11, 13-14, 22-24, and 26 are similarly patentable over Nakajima, Miremadi, and Moresco not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define.

Moreover, Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

V. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-4, 6-11, 13-14, 21-24, and 26 are patentably distinct over the prior art of record and are in condition for allowance. Therefore, the Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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